

Public Material- und Designrules for Working Group Microsystems, LTCC and HTCC

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1 Overview of Dielectric Base Materials

Type	HTCC			LTCC						
Description	44009	44007-G	42000-G	GT 951	9 k7	CT 702	Ferro L8	Ferro A6	41020	BGK
Manufacturer	ESL	ESL	ESL	DuPont	DuPont	Heraeus	Ferro	Ferro	ESL	IKTS
Composition	Al ₂ O ₃ (96 %)	Al ₂ O ₃ (99,9 %)	ZrO ₂ (3YSZ)	Corundum PbO ₂ -SiO ₂ - CaO-Glass	Corundum, B ₂ O ₃ , La ₂ O ₃ , CaO, P ₂ O ₅	Corundum, BaO- SiO ₂ -CaO-MgO- ZnO-Glass	Corundum, SiO ₂ -BaO- CaO-Glass	SiO ₂ -B ₂ O ₃ - CaO- Glass	Corundum SiO ₂ -BaO-CaO- ZnO-Glass	?
Available tape thicknesses in µm	200, 110	155	115	256; 165; 114; 51	127; 254	135 – 140	50,8; 127; 254	127; 254	100 - 130	50 - 250
Sintering temperature in °C	1500*	1550*	1450*	850*	850*	850 – 865*	850 – 900*	850*	850- 875*	850
Density green [fired] in g/cm ³	[3,6]*	[~ 3,7]*	(98 %TD)*	2,45* [3,1]*	[3,1]*	2,2 [3,2]*	2,3 [3,1]*	[2,5]*	[~ 3,2]*	[2,3]
TCE in ppm/K	~ 7,2*	~ 7,2*	10,5*	5,8*	4,4*	7,3*	5*	7*	7,4 (25...300°C)*	3,75
Heat conductivity in W/mK	~ 24*	~ 30*	~ 2*	2,6 – 3,3*	4,6*	4,3*	> 3*	2*	2.5-3.0*	1,5
Dielectric loss tanδ	?	?	?	0,006 (3 GHz)*	0,0009 (10 GHz)*	0,003 (1 kHz)*	0,002 (10 GHz)*	0,0010 (10 GHz)*	?	k. A.
Permittivity	~ 9 – 10 (1 MHz)*	~ 9 – 10 (1 MHz)*	≥ 20 (1 GHz)*	7,8 (3 GHz)*	7,1 (10 GHz)*	7,5 – 7,9 (1 KHz)*	7,3 (3 GHz)*	5,9 (10 GHz)*	7.0-8.5 (1 MHz)*	k. A.

(*Datasheet values)

2 Description of Material Systems

2.1 Dielectric Base Material DP951

Cofirable Pastes	Standard	R&D
Via	Ag, Au, AgPd (mixed metal)	AuAg (mixed metal)
Conductor		
Signal Line (internal)	Ag, Au)	Pt, Ag (coil structure M-Teck)
Signal Line (external)	Ag, Au	Pt (IKTS)
Ground Plane (innerlayer)	Ag	
Solderable	AgPd	
Resistor	RuO ₂ (10 , 100 Ohm; 1 , 10,5 kOhm)	RuO ₂
Encapsulating	glass	951-paste

Postfirable Pastes	Standard	R&D
Via/ Through hole		Ag
Conductor		
Termination	Au	
solderable	AgPd, AgPt, AuPdPt	
wire bondable		AgPt (silver coated Cu-wire)
Weldable		AgPt (silver coated Cu-wire)
Resistor	RuO ₂	RuO ₂
PTC	different types	
Encapsulating	glass	951-paste
Sealing glass	different types	different types

2.2 Dielectric Base Material 9k7

Cofirable Pastes	Standard	R&D
Via	Ag, Au	
Conductor		
Signal Line (internal)	Au, Ag	
Signal Line (external)	Au, Ag	
Ground Plane (innerlayer)		
Solderable	AuPt	
Resistor		in progress
Encapsulating		in progress

Postfirable Pastes	Standard	R&D
Conductor		
Termination		Au, AgPt, AgPt-Fineline
solderable		AgPt AgPt- Fineline
wire bondable		
weldable		
Resistor	RuO ₂	
PTC		in progress
Encapsulating		in progress
Sealing glass		in progress

3 Design Rules

3.1 General Rules

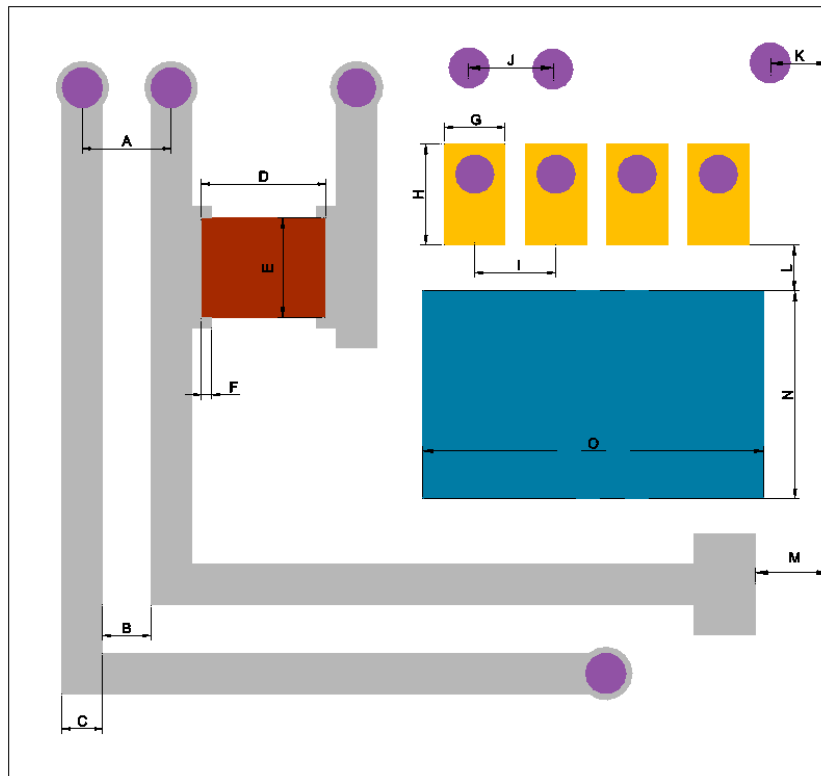


Fig. 1 Structural sizes for Top Layer elements

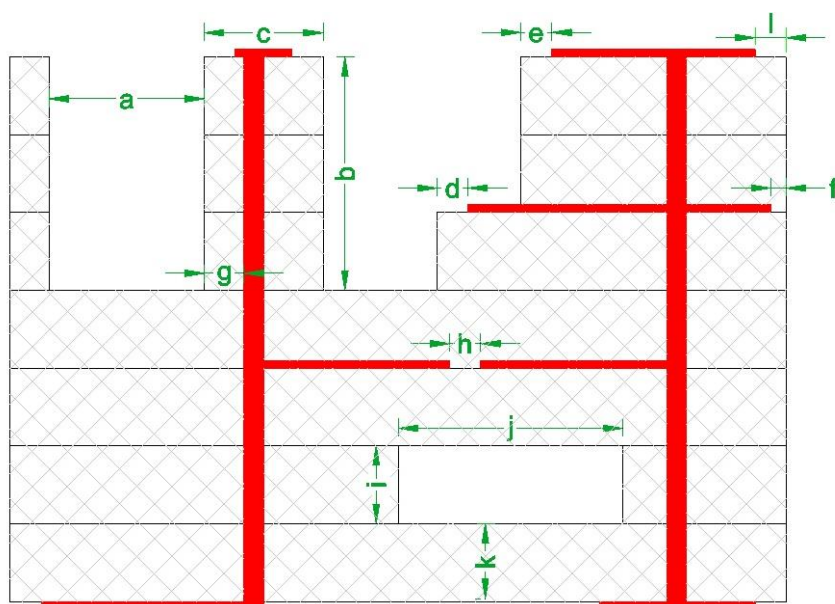


Fig. 2 Structural sizes in cross section

3.1.1 Dielectric Base Material DP951

General parameters	Unit	Standard	R&D
Substrate size	inch ²	green / fired □2 / □1,75 □4 / □3,5 □6 / □5,25 □8 / □7	
Registration hole diameter	mm	1; 2,24	
Usable area for circuits „Green“	mm	2 inch: 40x40 4 inch: 85x85 6 inch: 132x132 8 inch: 170x170	
Max. number of layers		1-25	>25
X,Y shrinkage	%	12,7 ± 0,3*	0,23 ± 0,02 (constrained sintering, 0,8 MPa)
Z shrinkage	%	15,5 ± 0,5*	40 (constrained sintering, 0,8 MPa)

(*Datasheet values)

Surface & Volume properties	Unit	Standard	R&D
Surface roughness (as fired)	nm [Ra]	≤ 600	≤ 300
Camber (warpage) (as fired)	mm/mm	0,2%-0,3%	<0,1%
Density green	g/cm ³	2,45*	
Density fired	g/cm ³	3,1*	
Percentage of theoretical density	%	96	


(*Datasheet values)

Basic structural sizes	No.*	unit	Standard (sintered)	R&D
Line pitch**	A	µm	200	80
Line spacing**	B	µm	100	40
Line width**	C	µm	100	40
Line thickness**		µm	1-12	20-40
Chip bond pad width	N	µm	>500	100
Chip bond pad length	O	µm	>500	100
Chip bond pad to feature	L	µm	200	50
Outer edge to feature	M	µm	250	50
Via diameter		µm	200	50
Via Spacing	J	µm	3x Via diameter	1x Via diameter
Via center to edge	K	µm	3x Via diameter	2x Via diameter
Via catch pad		µm	250	none
Maximum Via stack			3x	>10x
Pad width	G	µm	>200	100
Pad length	H	µm	>200	100
Pad pitch	I	µm	>300	200

(*Refer to Fig. 1; **depending on the printing technology)

Cavity structural sizes	No.*	Unit	Standard	R&D
Min. cavity width	a	μm	500	30
Min. cavity height	b	μm	100	10
Max. cavity width	a	mm	10	100
Max. cavity height	b	mm	1	10
Cavity bottom thickness	k	μm	250	30
Inner conductor cavity spacing	f	μm	250	100
Min. distance between cavities	c	μm	500	200
Via cavity spacing	g	μm	250	125
Cavity shelf edge-conductor spacing	d	μm	200	50
Min. inner channel width	j	μm	500	30
Min. inner channel height	i	μm	220	30
Top conductor-cavity spacing	e	μm	250	100
Distance substrate outer edge	l	μm	250	50
Distance inner layer conductor	h	μm	100	50

(*Refer to Fig. 2)

Resistor rules	No. *	Unit	Standard	R&D
Min. resistor dimension	E x D	mm	0,25 x 0,50	0,080 x 0,040
Min. resistor overlap	F	μm	100	50
Resistor geometry			rectangle	
Resistivity (postfired)		Ω/□	10*, 100*, 1* k, 10* k (Resistor, dried thickness 20μm)	
Resistivity (buried)		Ω/□	50 ± 5%; 170± 5%	10 kΩ/□ (tolerance t.b.d.)
Resistivity of inner layer conductors		mΩ/□	< 5* (Au, dried thickness 15μm) 5- 10 (Ag, dried thickness 15μm) 25- 30 (Ag/Pd, dried thickness 12μm) ~ 100 (Pt, dried thickness 8μm)	
Resistivity of outer layer conductors		mΩ/□	< 5* (Au, dried thickness 15μm) 5- 10 (Ag, dried thickness 15μm) < 60* (Ag/Pd, dried thickness 15μm) Pt k.A.	
TCR		ppm/K	0 to 50 2500 to 3300 (PTC)	
Gauge factor			1 to 12	
Long term stability		%	< 0,1 %R _{square}	1000 h/ 85°C/ 85 %HD
Tolerance as fired		%	< 10 %R _{square}	< 5 % R _{square}
Form of trim cut				
Value		%	> 150 %R ₀	
Tolerance after trimming		%	< 1%	

(*Refer to Fig. 1. **Datasheet values)

3.2 Rules for HF-Circuit Boards

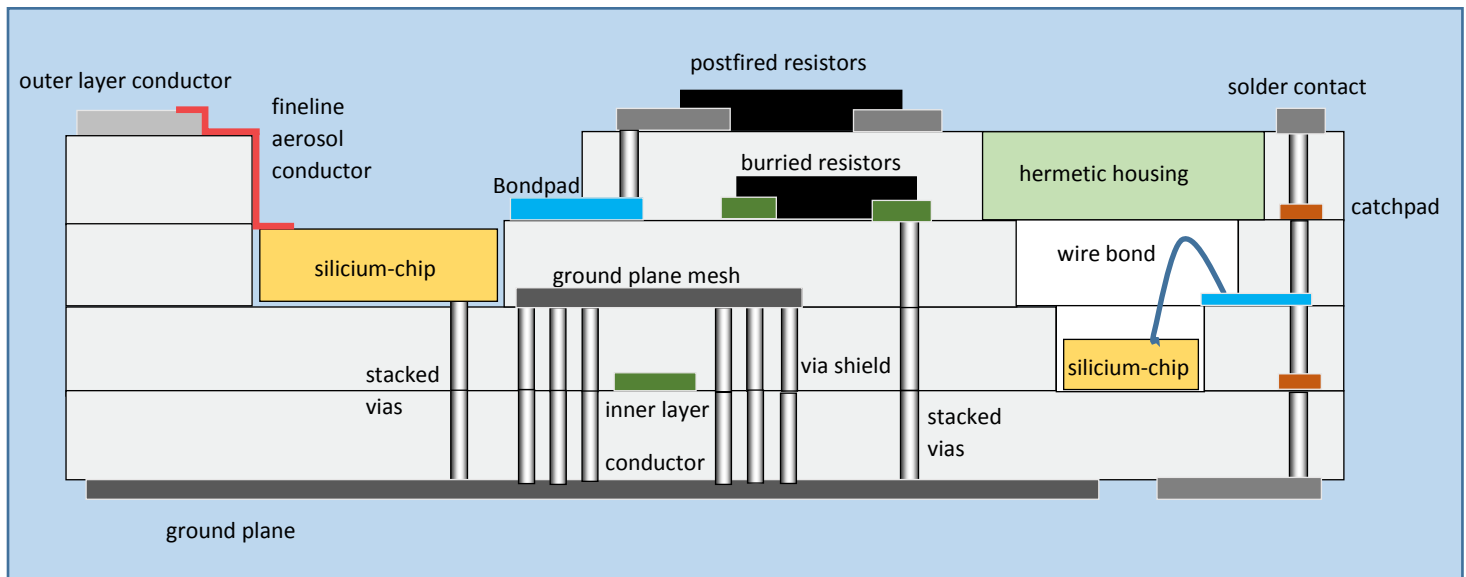


Fig. 3 Schematic for HF-Circuit board

3.2.1 High Frequency suited LTCC material

	Unit	Standard	R&D
Line/Space	μm	75 /75	15/20 (Aerosol Jet)
Printed Line tolerance	μm	± 10	± 2 (Aerosol Jet)
Isolating layer thickness	μm	50	20
Printed Layer thickness	μm	10-15 μm	3-15 μm
Ground layer		Grid	Entire substrate
Via diameter	μm	200	60
Via distance	μm	3 Via diameter	2 Via diameter
Surface roughness Ra			
- DuPont 9k7	nm	≤ 1200 (As-fired)	≤ 200 (polished)
- DuPont GT951	nm	≤ 600 (As-fired)	10-50 (polished)
- Ferro A6M	nm	≤ 1000 (As-fired)	≤ 100 (polished)

3.3 Rules for Power Electronic Circuit Boards

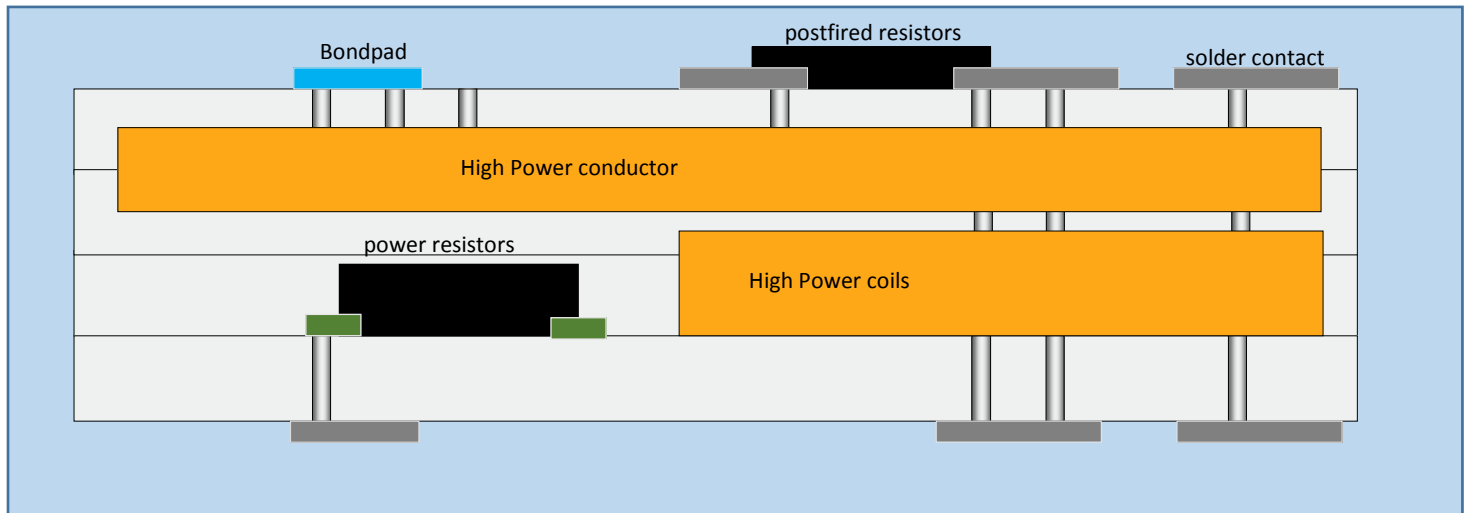


Fig. 4 Schematic for Power Electronic Circuit Board

3.3.1 Dielectric Base Material DP951

Power-Electronic	Unit	Standard	R&D
High Power conductor thickness (top)	μm	10- 15	300
High Power conductor thickness (buried)	μm	10- 15	150
High power resistor dimensions (DxE)	mm	0,5-5	> 5
High power resistor thickness	μm	20 μm	50 μm
High power resistor tolerance (buried)	%R	<10	<5
Resistor power dissipation	W/mm^2	2	>2
Thermal via diameter	μm	100-500	1000
Thermal via pitch	μm	3x Via diameter	2x Via diameter
Cover layer thickness	μm	43	20
Air/water cooling channels (i,j)	μm	50-1000	>1000
Thermal conductivity with vias	W/mK	20*	

(*Literature values)

3.3.2 Dielectric Base Material ESL 44009

Power-Electronic	Unit	Standard	R&D
high power postfired conductor thickness	μm	50	300
high power postfired resistor thickness	μm	20	50
Thermal via diameter	μm	500-1000	>1000
Thermal via pitch	μm	3x Via diameter	2x Via diameter
Thermal via coverage	%		
Cover layer thickness	μm	156	<100
Air/water cooling channels (ixj)	μm	50-1000	>1000
Thermal resistance with water cooling (R _{th})	K*cm ² /W	<0,5 (0,1 l/min H ₂ O, p _{loss} <0,1bar)	<0,3 (3 l/min H ₂ O, p _{loss} =0,75bar)
Break through voltage DC	Volt/μm		19,3
Break through voltage AC (50Hz)	Volt/μm		10,2

3.4 Rules for Ceramic Microsystems

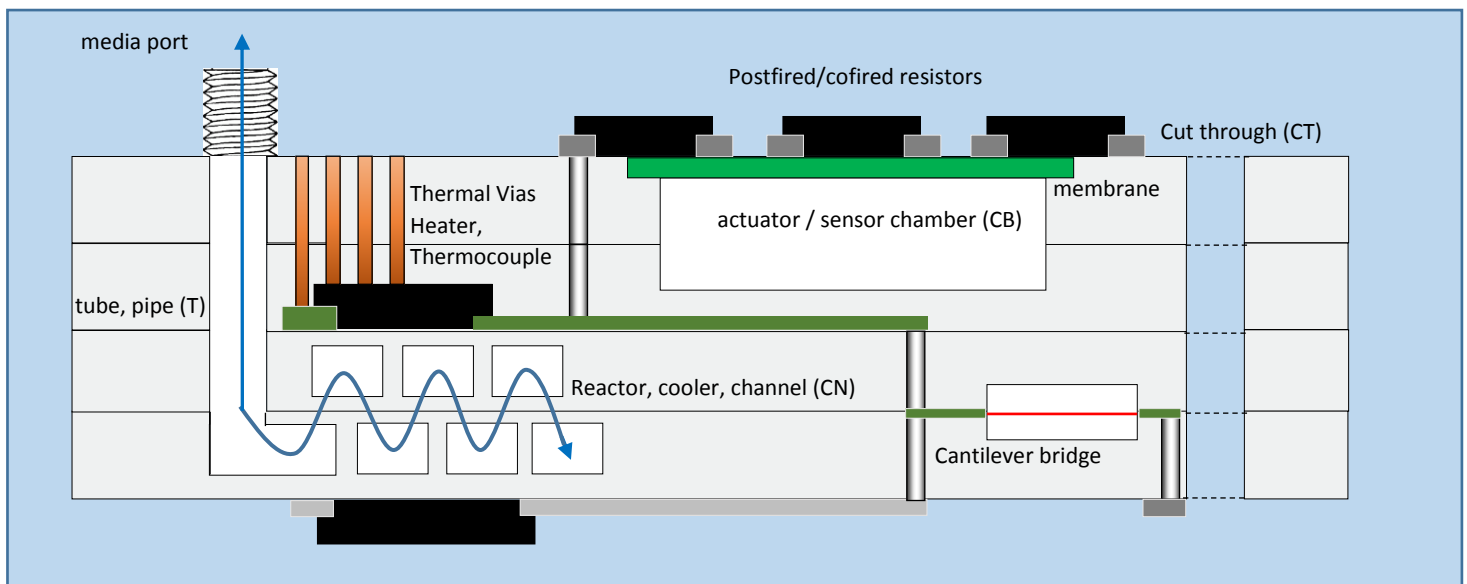


Fig. 5 Schematic for Ceramic Microsystem

3.4.1 Dielectric Base Material DP951

Sensor and Actuator, Energy, Reactor		Unit	Standard	R&D
Min. membrane thickness		μm	Tape thickness as fired	20
Max. membrane diameter		mm	5	10
Cut Out width (T, CB, CN, CT)	Min.	μm	50	10
	Max.	mm	5	10
Cut Out depth (T, CB, CN, CT)	Min.	μm	Tape thickness as fired	10
	Max.	mm	100-2000	>2000
media port				M5 thread
reactor channels diameter		μm	50-1000	>1000
Cantilever bridge width LTCC (Metallization)		μm		600 (150)
Cantilever bridge length		mm		4
Cantilever bridge thickness		μm		50